# SUBLITHOGRAPHIC CONTACT STRUCTURE, IN PARTICULAR FOR A PHASE CHANGE MEMORY CELL, AND FABRICATION PROCESS THEREOF

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a sub lithographic contact structure, in particular for a phase change memory cell, and a fabrication process thereof.

### Description of the Related Art

As is known, phase change memory cells utilize a class of materials that have the unique property of being reversibly switchable from one phase to another with measurable distinct electrical properties associated with each phase. For example, these materials may change between an amorphous disordered phase and a crystalline, or polycrystalline, ordered phase. A material property that may change and provide a signature for each phase is the material resistivity, which is considerably different in the two states.

At present, alloys of elements of group VI of the periodic table, such as Te or Se, referred to as chalcogenides or chalcogenic materials, can advantageously be used in phase change cells. The currently most promising chalcogenide is formed by a Ge, Sb and Te alloy ($Ge_2Sb_2Te_5$), which is currently widely used for storing information in overwritable disks.

In chalcogenides, the resistivity varies by two or more magnitude orders when the material passes from the amorphous phase (more resistive) to the polycrystalline phase (more conductive) and vice versa, as shown in Figure 1. Furthermore, in the amorphous phase, resistivity strongly depends also on temperature, with variations of one magnitude order every 100°C, with a behavior similar to that of P-type semiconductor materials.

Phase change may be obtained by locally increasing the temperature, as shown in Figure 2. Below 150°C both phases are stable. Above 200°C (temperature of start of nucleation, designated by $T_x$), fast nucleation of the crystallites takes place, and, if the material is kept at the crystallization temperature for a sufficient time (time $t_2$), it changes its phase and becomes crystalline. To bring the chalcogenide back into the amorphous state, it is necessary to raise the temperature above the melting temperature $T_m$ (approximately 600°C) and then to cool the chalcogenide off rapidly (time $t_1$).

From the electrical standpoint, it is possible to reach both critical temperatures, namely the crystallization and the melting temperatures, by causing a current to flow through a resistive element which heats the chalcogenic material by the Joule effect.

The basic structure of a PCM element 1 which operates according to the principles described above is shown in Figure 3 and comprises a first electrode 2 (of resistive type, forming a heater); a programmable element 3 and a second electrode 5. The programmable element 3 is made of a chalcogenide and is normally in the polycrystalline state after processing. One part of the programmable element 3 is in direct contact with the first electrode 2 and forms the active portion affected by phase change, hereinafter referred to as the phase change portion 4.

In the PCM element 1 of figure 3, technological and electrical considerations impose that the contact area between the first electrode and the programmable element has small dimensions, so that, for the same current density, the writing operation may be carried out at the required local thermal energy with smaller current consumption.

Several proposals have been presented for reducing the contact area. For example, US-A-6,294,452 discloses a process for forming a contact area of sublithographic dimensions, based on isotropically etching a polysilicon

layer. The resulting sublithographic dimensions depend on the quality of the etching.

US 2001/0002046 discloses a process for forming an electrode of a chalcogenide switching device, wherein a spacer layer deposited in a lithographic opening is anisotropically etched and laterally defines an electrode. The resulting width of the electrode depends on the thickness of a spacer layer.

U.S. patent application 10/313,991, filed on December 05, 2002, and entitled "Small Area Contact Region, High Efficiency Phase Change Memory Cell, And Manufacturing Method Thereof", teaches forming the contact area as an intersection of two thin portions extending transversely with respect to one another and each of a sublithographic size. In order to form the thin portions, deposition of layers is adopted.

In all the indicated prior solutions, any variation in the electrode width L (Figure 3), due for example to the process tolerances, affects, in a linear way, the contact area of the active region 4. Thus, the width L may have tolerances that are not acceptable as regards repeatability and uniformity of the cell characteristics.

## BRIEF SUMMARY OF THE INVENTION

An embodiment of the invention provides a contact region having an area less dependent on the process variations.

According to one aspect of the invention, the contact area is formed laterally to the active region and has a height and width. Advantageously, the height of the contact area is determined by the thickness of a deposited layer, which is technologically controlled and may be designed to be sublithographic. Furthermore, according to another aspect of the invention, the width of the contact area is determined by the width of a spacer which may also be designed of sublithographic dimensions and may be dimensionally controlled with a good accuracy.

## BRIEF DESCRIPTION OF THE DRAWINGS

For the understanding of the present invention, a preferred embodiment is now described, purely as a non-limitative example, with reference to the enclosed drawings, wherein:

Figure 1 illustrates the characteristic low field current-voltage of a phase change material;

Figure 2 shows the temperature versus time plot of a phase change material;

Figure 3 shows the basic structure of a PCM memory element;

Figure 4 shows a cross-section of a contact structure according to the present invention;

Figure 5 is a perspective view of a portion of the contact structure of Figure 4 showing the variability of the contact area due to technological tolerances;

Figure 6 is a cross-section of a PCM memory element in an initial manufacturing step;

Figures 7-11 are cross-sections of an enlarged detail of Figure 6, in subsequent manufacturing steps;

Figure 12 is a perspective view of the structure of Figure 11; and

Figures 13-16 are cross-sections of the PCM memory element, in subsequent manufacturing steps, taken in a perpendicular plane with respect to Figures 7-11.

## DETAILED DESCRIPTION OF THE INVENTION

Figure 4 illustrates the basic structure of a contact structure according to one embodiment of the invention. In detail, an electronic device 90 has a body 91 (*e.g.*, a substrate) of monocrystalline material defining an upper surface 92 and a lower surface 93 and accommodating electronic components 94, represented schematically. A dielectric layer 95 extends on top of the body 91 and accommodates the contact structure, indicated at 98. The contact structure 98 is

formed by a first electrode 100 and an active region 103 of chalcogenic material. The first electrode 100, connected to the electronic components 94 as shown schematically for one of them, has a horizontal portion 102 adjacent to and in contact with the active region 103. A second electrode 104 is formed on the active region 103 and is in electric contact therewith.

As better shown in the perspective view Figure 5, the horizontal portion 102 has an elongated shape extending along a longitudinal direction X parallel to the upper and lower surfaces 92, 93 of the body 91. The horizontal portion 102 is longitudinally delimited by an end face 110. The end face 110 extends in a vertical plane, which is ideally perpendicular to the longitudinal direction X and thus to the upper and lower surfaces 92, 94 and defines a lateral contact area with the active region 103. The end face 110 is here rectangular and has a height S (extending parallel to direction Z) and a width W (extending parallel to direction Y). The portion of the active region 103 adjacent to the end face 110 undergoes phase change and thus corresponds to the active region 4 of Figure 3.

Because of the vertical arrangement of the end face 110 and thus of the contact area, the height S is equal to the thickness of the horizontal portion 102 of the first electrode 100, and thus may be designed to be sublithographic, that is smaller than the minimum dimension obtainable through optical UV lithography.

In practice, the contact structure 98 according to Figures 4, 5 is formed by an elongated formation (horizontal portion 102 of the first electrode 100) having a longitudinal extension parallel to the upper surface 92 of the body 91 and an end face 110 extending in a vertical plane and in contact with the active region 103 so that the dimensions of the contact area (defined by the end face 110) are determined by the thickness S of the elongated formation and by the width W thereof.

The height S of the horizontal portion 102 and thus of the contact area is more controllable than the electrode width L of prior art contact structures (Figure 3), so that PCM cells having the contact structure of Figure 4 have more

uniform dimensions than prior art cells. The thickness tolerance of a conductive layer forming the horizontal portion 102 allows, for same overall dimensions, a higher constructive confidence than electrodes the contact area whereof depends on the width L.

The height S also depends on the quality of the operation used to define the end face 110, in particular by the etching operation used to this end. Figure 5 shows the possible variation of the contact area in case etching does not ensure exact verticality of the end face 110, so that horizontal portion 102 has an inclined end face, indicated at 110', forming an angle $\alpha$ with ideal end face 110 (which, as said, is perpendicular to the upper surface 92). In this case, the height S' of the inclined end face 110' is greater than height S by a quantity depending on the angle $\alpha$, since

$$S' = S/\cos\alpha.$$

In the worst cases, with current technologies, $\alpha \leq 5°$, so that $\cos\alpha \cong 1$ [cos(5°)=0.99619]. Since any variation of height S has the same impact on the contact area, the variation of the contact area due to process tolerances affecting the height S is lower than 2%.

Furthermore, also the width W may be sublithographic, by exploiting the spacer technique, as discussed later on, with reference to Figures 7-12. This technique has a tolerance of ±10%.

The process for manufacturing the contact structure of Figure 4 will be now described, with reference to Figures 6-16.

First, Figure 6, a wafer 10 comprising a P-type substrate 11 having an upper surface 16 is subjected to standard front end steps. In particular, inside the substrate 11 insulation regions 12 are formed and delimit active areas; then, in succession, base regions 13 of N-type, base contact regions 14 of $N^+$-type, and emitter regions 15 of $P^+$-type are implanted. The base regions 13, base contact regions 14, and emitter regions 15 form diodes or bipolar transistors that define selection elements for the memory cells.

Next, a first dielectric layer 18 is deposited and planarized; openings are formed in the first dielectric layer 18 above the base contact regions 14 and emitter regions 15, and the openings are filled with tungsten to form emitter contacts 19a and base contacts 19b. Then, a second dielectric layer 20 -for example, an undoped silicon glass (USG)- is deposited, and openings 21, for example, cylindrical-shaped, are formed in the second dielectric layer 20 above the emitter contact 19a. Next, a cup-shaped region 22 is formed, *e.g.,* by depositing an electrode layer, for example of TiSiN, TiAlN or TiSiC, that conformally coats the walls and bottom of the openings 21, a dielectric material is then deposited filling the openings 21, and then the dielectric material and electrode layer are subsequently removed outside the openings 21, using conventional planarization techniques such as Chemical Mechanical Polishing (CMP). The cup-shaped region 22 thus has a vertical wall 22a extending along the cylindrical side surface of the openings 21.

Then, a conductive layer 27 (for instance TaSiN, TiSiN, TiN, TiAlN, etc.) having a thickness of 5-50 nm, corresponding to the desired height S of the contact area 110 is deposited, thus obtaining the structure of Figure 6. As visible, the conductive layer 27 extends parallel to the upper surface 16 of substrate 11.

At this point, a mask is exposed and the conductive layer 27 is selectively etched in order to form stripes parallel to the y-direction.

The width of these stripes has to be enough to ensure that the strips touch the conductive ring formed by the vertical walls 22a on one side and be cut by the trench etch described inFigure 14 on the other side.

Next, Figure 7, a delimiting layer 29 of insulating material, for example oxide, is deposited. The delimiting layer 29 has a thickness of, for instance, 20-200 nm. Then, using a mask, one part of the delimiting layer 29 is removed by dry etching to form a step which has a vertical side 29a that extends vertically on top of the dielectric material 23, and crosses the vertical wall 22a of

cup-shaped region 22 (at a point located before or behind the drawing plane, and thus not visible in Figure 7).

Next, a sacrificial layer 28, for example nitride with a thickness of 5-50 nm, is deposited conformally. In particular, the sacrificial layer 28 forms a vertical wall 28a that extends along the vertical side 29a of the delimiting layer 29. Thus, the structure of Figure 7 is obtained.

Thereafter (Figure 8), the sacrificial layer 31 undergoes an anisotropic etching that results in removal of the horizontal portions of the sacrificial layer 28 and of part of the vertical wall 28a. By appropriately choosing the thickness of the delimiting layer 29 and the thickness of the sacrificial layer 28, as well as the time and type of etching, it is possible to obtain the desired sublithographic width W for the bottom part of the remaining vertical wall 28a.

Then, Figure 9, the remaining portion of the delimiting layer 29 is removed and, Figure 10, using the vertical wall 28a as a hard mask, the conductive layer 27 is defined. Thereafter, Figure 11, the vertical wall 28a is removed.

Now, as shown in perspective in Figure 12, the remaining portion of the conductive layer 27 (strip-shaped portion 27a) has a height S and a width W.

Thereafter, Figure 13, an insulating layer 30 (*e.g.*, silicon oxide) and an adhesion layer 31 (*e.g.*, Si, Ti, Ta, etc.) are deposited in sequence.

Then, Figure 14, a trench 32 of lithographic dimensions is opened. The trench 32 is an aperture having a preset length in the direction perpendicular to the drawing sheet, intersects the strip-shaped portion 27a and extends within the second dielectric layer 20 so as to longitudinally delimit the strip-shaped portion 27a. In practice, the trench 32 determines the length L1 of the strip-shaped portion 27a.

Thereafter, Figure 15, a chalcogenic layer 33, for example of $Ge_2Sb_2Te_5$ having a thickness of *e.g.*, 20-200 nm, is conformally deposited and fills

the trench 32 with a reduced area portion 33b the shape and dimensions whereof are determined by the trench 32.

Then, a barrier layer 34, for example of Ti/TiN, and a metal layer 35, for example of AlCu, are deposited in sequence on top of the chalcogenic layer 33; the stack formed by the metal layer 35, the barrier layer 34 and the chalcogenic layer 33 is defined using a same mask, thus forming a bit line 41 including a chalcogenic region 33a and metal regions 34a, 35a. Finally, a third dielectric layer 42 is deposited, which is opened above the base contacts 19b. The openings thus formed are filled with tungsten to form top contacts 43 in order to prolong upwards the base contacts 19b. Then standard steps are performed for forming connection lines in contact with the top contacts 43 and with the bits lines 41, pads are formed and a passivation layer 45 is deposited, defining a device main surface 46. Thus, the final structure of Figure 16 is obtained.

In practice, the strip-shaped portion 27a (corresponding to the horizontal portion 102 of the first electrode 100 of Figure 4) has a longitudinal extension parallel to upper surface 16 of the substrate 11 and forms, with the bottom portion of the reduced area portion 33b, a contact area the height whereof is defined by the thickness of the conductive layer 27 and the width whereof is defined by the thickness of the sacrificial layer 28. The quality of the etching of trench 32 determines the orientation of the contact area with respect to the upper surface 16.

The advantages of the present invention are clear from the above. In particular, it is outlined that the present contact structure has a very good technological repeatability, a lower dependence from the process variations than prior art solutions, while maintaining a very small contact area, having sublithographic dimensions in both directions.

Finally, it is clear that numerous variations and modifications may be made to the contact structure and process described and illustrated herein, all falling within the scope of the invention as defined in the attached claims.

In particular, it is stressed that the direction of the horizontal portion 102 and the conductive layer 27 is defined with reference to the upper surface 92, 16 of the substrate, intending therewith a plane corresponding to the original upper surface of the wafer. In practice, the horizontal portion 102 and the conductive layer 27 are perpendicular to the direction of growing of the substrate, due to the deposition of the various superficial layers. If, due to deposition, thermal growing, etching and implant steps carried out on the wafer, the upper surface 16 of the finished device is no more planar, reference may be done to the lower surface 93 of the substrate or to the device main surface 46.

Moreover an alternative embodiment of the present invention provides that the conductive layer 27 is in direct contact with the emitter layer 19a, thus avoiding the dielectric layers 20 and 23 and the cup-shaped region 22.

All of the above U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet are incorporated herein by reference, in their entirety.